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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,581	07/22/2003	Isamu Kobori	07977-024003	6534

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EXAMINER

ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
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2812

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/623,581

Applicant(s)

KOBORI ET AL.

Examiner

Stanetta D. Isaac

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-36 and 46-60 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-36 and 46-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>5/02/06 & 1/12/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the RCE filed on 5/02/06. Currently, claims 16-36 and 46-60 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 5/02/06 has been entered.

Information Disclosure Statement

The information disclosure statements (IDS) were submitted on 5/02/06 and 1/12/07. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 16-19, 21-25, 27-33, 46-48, 50-53-58 and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al., US Patent 6,198,133

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Yamazaki discloses the semiconductor method as claimed. See figures 1-11D, and corresponding text where, Yamazaki teaches, pertaining to claims 16, 22 and 28, a method for forming an active matrix circuit comprising a transistor, said method comprising: doping a p-type impurity 619-620 into a semiconductor layer 603-605 by ion doping to form a p-type impurity region in said semiconductor layer, said semiconductor layer comprising a part to become a channel region adjacent to said p-type impurity region (figure 6E; col.7, lines 64-67; col. 8, lines 1-5); forming a gate electrode 609/611 adjacent to said part to become said channel region (figure 6A; col. 7, lines 20-23); activating said p-type impurity by annealing (figure 6E;

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col. 8, lines 17-21); and forming an interlayer insulating film **622** comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said semiconductor layer (figure 6F; col. 8, lines 23-27); and forming a conductive multi-layer film, comprising a titanium layer and an aluminum layer over said interlayer insulating film, wherein said transistor of said active matrix circuit comprise said channel region and said gate electrode and said p-type impurity region (figure 6G; col. 8, lines 28-31).

Yamazaki teaches, pertaining to claims 17, 23 and 31, wherein said active matrix circuit is incorporated into a liquid-crystal device (col. 1, lines 12-20 conventional devices).

Yamazaki teaches, pertaining to claims 18, 24 and 32, wherein said active matrix circuit is incorporated into an image sensor (col. 1, lines 62-67; col. 2, lines 1-7 conventional devices that include image sensors).

Yamazaki teaches, pertaining to claims 19, 25 and 33, wherein said active matrix circuit is incorporated into a liquid crystal electro-optical device (col. 1, lines 12-20 conventional devices).

Yamazaki teaches, pertaining to claims 21, 27 and 35, further comprising crystallizing said amorphous semiconductor island (figure 6A; col. 6, lines 50-67; col. 7, lines 1-5).

Yamazaki teaches, pertaining to claim 29, wherein said conductive layer comprises an electrode (figure 6A; 7, lines 20-24).

Yamazaki teaches, pertaining to claim 30, wherein said conductive layer comprises a wiring (figure 6G; col. 8, lines 27-37).

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Yamazaki teaches, pertaining to claim 36, wherein said conductive layer comprises a multi-layer film including a titanium layer and an aluminum layer (figure 6G; col. 8, lines 27-31).

Yamazaki teaches, pertaining to claims 46, 51 and 56, a method for forming an active matrix circuit comprising a transistor, said method comprising: doping a p-type impurity 619-620 into a semiconductor layer by ion doping to form a source region and a drain region in said semiconductor layer, said semiconductor layer 603-605 comprising a part to become a channel region between said source region and said drain region (figure 6E; col.7, lines 64-67; col. 8, lines 1-5); forming a gate electrode 609-611 adjacent to said part to become said channel region (figure 6A; col. 7, lines 20-23); activating said p-type impurity by annealing (col. 8, lines 17-21); forming a first interlayer insulating film comprising a silicon nitride layer and a silicon oxide layer over said semiconductor layer by plasma CVD, said silicon nitride layer and said silicon oxide layer formed over said gate electrode and said semiconductor layer (figure 6F; col. 8, lines 23-27); forming a conductive layer comprising a titanium and an aluminum over said first interlayer insulating film (figure 6G; col. 8, lines 28-31); forming a second insulating film comprising silicon oxide 632 over said conductive layer (figure 6G; col. 8, lines 31-33); and forming a pixel electrode 633 over said second insulating film, wherein said transistor of said active matrix circuit comprises said channel region and said gate electrode and said source region and said drain region (figure 6G; col. 8, lines 33-36).

Yamazaki teaches, pertaining to claims 47, 52, and 57, wherein said active matrix circuit is incorporated into a liquid crystal display (col. 1, lines 12-20 conventional devices).

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Yamazaki teaches, pertaining to claims 48, 53 and 58, wherein said active matrix circuit is incorporated into an image sensor (col. 1, lines 62-67; col. 2, lines 1-7 conventional devices that include image sensors).

Yamazaki teaches, pertaining to claims 50, 55 and 60, further comprising crystallizing said amorphous semiconductor island (figure 6A; col. 6, lines 50-67; col. 7, lines 1-5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 20, 26, 34, 49 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable Yamazaki et al., US Patent 6,198,133.

Yamazaki discloses the semiconductor method substantially as claimed. See preceding rejection of claims 16-19, 21-25, 27-33, 46-48, 50-53-58 and 60 under 35 U.S.C. 102(e).

However, Yamazaki fails to show, pertaining to claims 20, 26, 34, 49 and 54, a method, wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of $1000 \mu\text{m}^2$ or less.

Yamazaki teaches, a plurality of thin film transistors used in the formation of an active matrix circuit device (figures 6G; col. 8, lines 35-41).

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein said semiconductor layer comprises an amorphous semiconductor island having a plane area of $1000 \mu\text{m}^2$ or less, pertaining to claims 20, 26, 34, 49 and 54, in the method of Yamazaki,

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according to the teachings of Yamazaki, with the motivation that, the conventional active matrix circuits, taught by Yamazaki, generally include a plurality of thin film transistor devices used as a driving circuit, where these transistors are formed on semiconductor islands. Therefore, forming an amorphous semiconductor island having an area of $1000\text{-}\mu\text{m}^2$ or less, are parameters of optimization, where one of ordinary skill in the art would be capable of forming a desired area of the amorphous semiconductor island during routine experimentation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
January 20, 2007


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER